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Evaluation of Light-Triggered Thyristors for Pulsed Power Applications

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Abstract - Lawrence Livermore National Laboratory has many needs for high reliability, high peak current, high di/dt switches. Solid-state switch technology offers the demonstrated advantage of reliability under a variety of conditions. Light-triggered switches operate with a reduced susceptibility to electromagnetic interference commonly found within pulsed power environments. Despite the advantages, commercially available solid-state switches are not typically designed for the often extreme pulsed power requirements. Testing was performed to bound the limits of devices for pulsed power applications beyond the manufacturers' specified ratings. To test the applicability of recent commercial light-triggered solid-state designs, an adjustable high current switch test stand was assembled. Results from testing and subsequent selected implementations are presented.

I. Introduction

In pulsed power system design, the switch is arguably the most critical fundamental element. Reliable switching is essential to the performance of the system. Solid-state switch technology offers the demonstrated advantage of reliability under a variety of conditions. Light-triggered switches operate with a reduced susceptibility to electromagnetic interference commonly found within pulsed power environments. Despite the advantages, commercially available solid-state switches are typically not designed for the often extreme pulsed power requirements.

Solid-state switching is the future direction for many pulsed power applications with high-current, high-energy capacitor discharge units. Lawrence Livermore National Laboratory (LLNL) has many switching needs including magnetic flux compression generators, flashlamp banks, pulsed high-field magnets, compact electric power conversion, and electromagnetic launchers.

High current switching poses a unique set of challenges. This effort focused on two key switch characteristics: high peak current and high di/dt. High peak current handling capability decreases the number of parallel switches, thus reducing cost and system complexity. High di/dt capability increases the range of possible loads to the system. Both criteria are important for pulsed power switch selection.

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TABLE I
SELECTED DEVICE CHARACTERISTCS [1],[2]

Rated Value	Eupec T553N	Eupec T2563NH
Peak Voltage	7 kV	8 kV
Surge Current (10 ms)	12 kA	93 kA
Non-periodical di/dt	1 kA/μs	5 kA/μs
Action	$732 \times 10^{3} \text{ A}^{2}\text{s}$	$43250 \times 10^3 \text{ A}^2\text{s}$
Conducting Diameter	5.5 cm	12 cm

To determine the suitability of light-triggered thyristors for pulsed power applications beyond manufacturers' ratings, devices were stressed beyond the di/dt rating while maintaining low peak currents and, conversely, stressed beyond the peak current rating while maintaining a low current rate of rise. The chosen devices with selected characteristics are outlined in Table 1.

II. 12 kA, 1 kA/µs DEVICE TESTING

A. Trigger Pulse Testing

In phase control applications utilizing the Eupec T553N, the manufacturer recommends a square trigger pulse of 0.8 A for a duration of 12 μs . Holding the peak diode current at the rated 0.8 A, the pulsewidth was decreased from 12 μs to 6 μs , 3 μs , and 1 μs for trigger pulse testing. Very little effect was noted until the pulse was narrowed to 1 μs . With a 1 μs pulsewidth, the delay in onset of device current increased by 30% with a pronounced increase in jitter. However, an increase in drive current to 1 A with the 1 μs pulsewidth improved both delay and jitter.

Maintaining the recommended 12 μ s pulsewidth while decreasing the laser diode current from 1 A to 0.55 A provided information on the sensitivity to laser diode current level. As diode current was decreased, minimal effect was noted until it reached 0.65 A. Below 0.65 A, the delay and jitter increased rapidly. At current levels below 0.55 A, the device did not trigger. Trigger current amplitude appeared to have a greater impact than pulsewidth on device triggering.

B. High di/dt Testing

Initial high di/dt testing of the T553N device consisted of a floating 5 μF capacitor switched into a 2.5 Ω resistive load as seen in Fig. 1. With a 5 kV charge voltage, the circuit developed a peak current of 1.7 kA at 1.85 kA/ μs . The system was operated at 1 Hz for approximately one hour at 5 kV, or approximately 3600 shots.

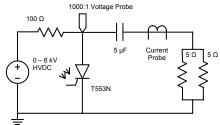


Fig. 1. Initial pulse test circuit.

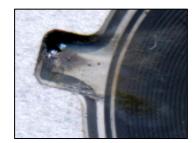


Fig. 2. Image of T553N failure.

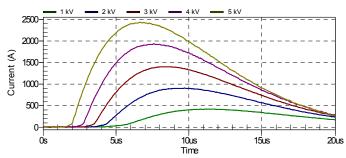


Fig. 3. Delay in current onset with decrease in voltage.

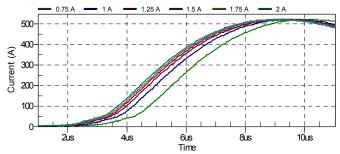


Fig. 4. Improved current turn-on time with increase in laser-driver current.

The load resistance was then reconfigured to provide a $1.25~\Omega$ resistive load. At 5 kV, the peak current reached 3 kA with a peak di/dt of $2.24~\text{kA/\mu s}$. The thyristor failed after approximately 15 minutes of operation at 1 Hz.

The failure of the thyristor was likely due to excess di/dt. For the T553N device, Eupec specifies a maximum non-periodical di/dt of 1 kA/µs or 300 A/µs at 50 Hz. A dissection of the failed thyristor revealed a single point of damage at the edge of the optical gate structure (see Fig. 2).

A second T553N was tested and the test circuit was modified to limit the di/dt to less than 1 kA/μs by adding approximately 2 μH of inductance. Twenty-five feet of RG-

213U cable was added in series with the 1.25 Ω load resistor. Peak device current at 5 kV was 2.5 kA and peak di/dt was 884 A/ μ s. The device failed after about 15 minutes at 1 Hz operation. Physical inspection of the device revealed a failure identical in appearance to the first unit.

C. Improved Gate Drive

It was noted that as the anode voltage across the device was decreased, the time to onset of current flow increased (see Fig. 3). In a conventional thyristor, an increased gate current may improve this timing. Throughout the previously mentioned testing, the current output from the laser diode driver was limited to approximately 1 A. The laser diode driver was later modified to provide up to a 2 A current pulse. A test was conducted by increasing the drive current from 0.75 A to 2.0 A in 0.25 A steps (see Fig. 4). Subsequently, nominal operating values for laser diode driver current were established at 2 A with a 5 µs pulsewidth.

D. Magnetically-Assisted Switching

In an effort to improve the switching performance of the Eupec T553N device, the addition of a series saturable inductor was explored. Several potential benefits to magnetically-assisted switching exist: 1) the rise/fall time of the circuit may improve, 2) less energy may be deposited in the switch, allowing for higher repetition rates and 3) the associated delay in the onset of high current may allow the device to more fully turn on, allowing for improved peak current and higher di/dt.

The T553N did not respond as expected when coupled with a saturable inductor. The current through the device was similar to electrically-triggered devices with about 500 ns of delay and a sight decrease in peak current (Fig. 6). The voltage waveform was completely unforeseen (Fig. 7). As expected, the voltage fall time was more rapid and deeper than for the unassisted case. However with the onset of current flow, the voltage across the device increased rapidly, indicating that the thyristor was still quite resistive.

In a conventional thyristor, the magnetically-induced delay allows for the entire device to turn on before the current begins to rise, resulting in a more uniform distribution of current and a lower on-resistance. The light-triggered thyristor behaves differently due to an integrated resistor built into the optical gate structure to limit gate currents. The manufacturer states that the di/dt of the device is dependent on this resistance. Delaying the onset of current flow did not improve the performance of these devices.

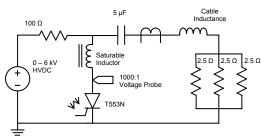


Fig. 5. Magnetic-assist test circuit.

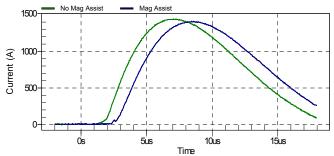


Fig. 6. Magnetic-assist current turn-on time comparison.

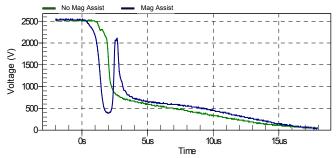


Fig. 7. Magnetic-assist voltage turn-on time comparison.

E. Parallel Operation for High Peak Current Testing

Parallel operation of the Eupec T553N devices was explored as a way to improve peak current performance. Fig. 8 describes the test circuit. Initially, the balance transformer was omitted and the devices were connected directly in parallel. The timing of the two optical triggers was carefully adjusted to coincide within 10ns. In this state, the current balance was not satisfactory with one device carrying almost twice the current as the other. At 5 kV, the total peak current was obtained with one device carrying 930 A (36%) and the other device carrying 1531 A (64%).

A bifilar transformer was constructed with 9 turns each of #16 high voltage wire on a PE11B ferrite core. At 5 kV, the peak current fell by 3.3% due to the increased series inductance introduced by the transformer. Little improvement in current sharing was noted (39% and 61%). As an increase in transformer turns may enhance current sharing, the corresponding increase in series inductance limits the peak current and di/dt.

Additionally, it was noted that turn-on time between the devices varied considerably. The timing between the optical triggers was adjusted to force the two devices to turn on at nearly the same time. The improvement in current sharing was dramatic. As expected, peak current was not affected but the current-carrying ratio improved significantly (46% and 54%). This leads to a possible active solution to the current sharing issue without the losses associated with a series transformer.

III. 93 kA, 5 kA/μs DEVICE TESTING

Switch testing of the higher current device, Eupec T2563NH, was conducted in two customizable test beds. A resistive load was implemented for high di/dt testing while

maintaining low peak current. An inductive load was constructed for high peak current testing while maintaining low di/dt. Each load consisted of a variable number of resistors and inductors, respectively, to target the bounds of operation for the device. During testing, full pulsewidth was minimized to less than 10% of nominal 10 ms rating. Switch action was kept orders of magnitude below specified rating.

A. High di/dt Testing

The resistive load for high di/dt testing was composed of ten parallel 0.25 Ω disc resistors. Connection bars of various lengths were fabricated to allow for resistance values from 25 $m\Omega$ to 125 $m\Omega$. The inductance of the circuit was 650 nH. Fig. 9 outlines the circuit.

During high di/dt testing between 5.6 to 7.2 kA/µs, the device failed after four shots operating above the datasheet rated di/dt despite minimal current injection of 28 to 36 kA. In high di/dt testing, the majority of the failures were located between the third and fourth amplifying gates (Fig. 11). Previous publications indicate that the location of a resistor in the amplifier gate (AG) structure allows for di/dt rates up to 10 kA/µs for single pulse applications and 5 kA/µs for periodical 60 Hz operation [3]. The pulse repetition rates tested at LLNL were approximately one shot per five minutes and the single pulse di/dt rating did not appear to increase from the periodical rating.

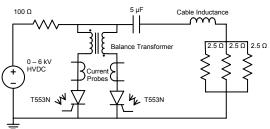
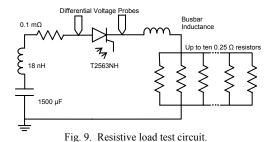


Fig. 8. Parallel operation test circuit.



Differential Voltage Probes
Busbar Inductance
Up to nine 9 μH, 33 mΩ inductors
T2563NH

1500 μF

Diode Stack

Fig. 10. Inductive load test circuit.

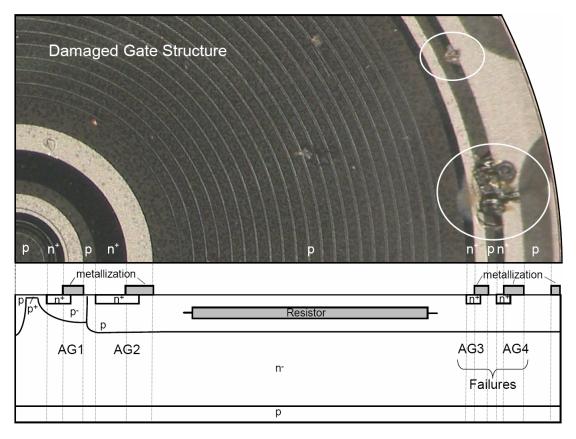


Fig. 11. Perceived location of T2563NH Amplifier Gate (AG) failures during high di/dt testing [4].

B. High Peak Current Testing

The inductive load for high peak current testing was composed of nine parallel 9 μ H, 33 m Ω inductors. Due to the size and weight of the inductors, dielectric connection pieces were fabricated to electrically, not physically, remove inductors from the circuit. The circuit is described in Fig. 10.

High peak current testing indicated failure eminent at currents slightly over rated values. Failures were occurring at 95 kA with the datasheet rated value of 93 kA. These failures were developing despite the low di/dt of 1.6 kA/µs and FWHM pulsewidth of approximately 300 µs. Although previous publications indicate a peak current performance of 126 kA for a surge current of 700 µs, the survival limit of the devices appeared to be closer to 90 kA peak [3].

Additionally, the optical trigger pulsewidth was optimized such that no observable decrease in turn-on time could be achieved. The trigger pulse amplitude was also maximized until driver-board limited at 3.6 A. The decrease in power dissipated by the switch due to the slight reduction in device turn-on time appeared to reduce the magnitude of destruction evident during dissection post-mortem. However, no increased peak current carrying ability was demonstrated due to modification of the trigger pulse. Water-cooling was also investigated, but no observable benefit was achieved.

IV. SUMMARY

For high reliability, we have concluded that the tested devices should not be operated outside of the specified ratings

despite a significant decrease in pulsewidth. With the current state of the technology, light-triggered solid-state switches may be self-limiting for demanding high current pulsed power applications. The increased cost and complexities introduced with series or parallel combinations to achieve operation within ratings may prove too cumbersome for some high current applications in the near future.

Within the specified ratings, the devices provide a demonstrated advantage of reliability. Light-triggered switches operate at a potential further advantage with a reduced susceptibility to electromagnetic interference commonly found within pulsed power environments. If the optical gate technology advances towards higher peak current and higher di/dt levels, the pulsed power community may serve to benefit.

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